A Modular Multilevel DC/DC Converter With Fault Blocking Capability for HVDC Interconnects

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***Abstract*—This paper introduces a modular multilevel dc/dc converter, termed the DC-MMC, that can be deployed to interconnect HVDC networks of different or similar voltage levels. Its key features include: 1) bidirectional power flow; 2) step-up and step-down operation; and 3) bidirectional fault blocking similar to a dc circuit breaker. The kernel of the DC-MMC is a new class of bidirectional single-stage dc/dc converters utilizing interleaved strings of cascaded submodules. The DC-MMC operation is analyzed and an open loop voltage control strategy that ensures power balance of each submodule capacitor via circulating ac currents is proposed. Simulations performed in PLECS validate the DC-MMC's principle of operation and the proposed control strategy. Experimental results for a 4-kW laboratory prototype illustrate the single-stage dc/dc conversion process for both step-down and step-up operating modes.**

***Index Terms*—Converters, dc-dc power conversion, HVDC converters, multilevel systems.**

I. Introduction

DC transmission is rapidly becoming a preferred choice for the large-scale integration of renewable energy sources [1]. Most notably, its potential benefits for grid connection of offshore wind farms are widely recognized [2]–[8]. Due to this changing electrical landscape, the development of dc grids for the collection and distribution of energy from renewable sources is gaining traction [9]–[11]. Utilizing HVDC technology as the backbone for such applications has recently garnered significant attention [12]–[14].

Although the prospect of HVDC-based grids offers many benefits, one of the principle challenges facing their widespread deployment is the interconnection of different dc networks and management of power flows between them. To accommodate both functions, bidirectional dc/dc converters can be dispatched [15]–[17] (although other devices tailored for power flow control exist [15], [18]). By using dc/dc converters to adjust line voltages, or the voltage between different network segments, the power controllability within dc grids can be extended [19]. Furthermore, formation of larger dc networks can be realized by utilizing dc/dc converters to mesh together smaller preexisting dc grid segments. However, due to the high-voltage (i.e., hundreds of kilovolts) and high-power (i.e., hundreds of megawatts) requirements, few dc/dc topologies are suitable for HVDC applications. The use of two cascaded dc/ac stages [16], [20]–[22] is costly and hinders overall conversion efficiency while transformerless dc/dc converters are typically not fully modular [23]–[26] and can suffer from uncontrolled propagation of fault currents [26] due to external dc faults.

Due to its modular structure and many operational advantages, the well-known modular multilevel converter (MMC) [27]–[30] has become a preferred solution for dc/ac conversion in various power system applications. The MMC is particularly attractive for use in HVDC transmission [11], [31]–[34], where its scalable architecture enables large operating voltages to be realized by simply stacking the requisite number of submodules (SMs) in cascade. However, the main drawback of MMC-based dc/dc topologies is that they require two cascaded dc/ac conversion stages [16], [21], [22]. This is a relatively costly solution as each dc/ac stage must process the same input power, resulting in poor utilization of total installed SM rating. Moreover, the inherent need for an intermediate ac link and transformer rated for the full input power further adversely impacts the total cost as well as overall conversion efficiency.

This paper proposes a modular multilevel dc/dc converter, termed the DC-MMC, that has the capability to interconnect HVDC networks of either different or similar voltage levels while simultaneously offering the promise of bidirectional fault blocking. The DC-MMC uses multiple interleaved strings of cascaded SMs to perform single-stage bidirectional dc/dc conversion, and is capable of both step-down and step-up operation. Elimination of the traditional intermediate ac link is achieved by exploiting circulating ac currents to maintain power balance of each SM capacitor. This new energy conversion process employs a power transfer mechanism first introduced in [35], which bears similarity to that recently described in [36]. A significant advantage of the DC-MMC is that a single converter structure can be utilized in place of two cascaded dc/ac converters. This offers a substantial improvement in utilization of total installed SM rating, as all SMs within the DC-MMC contribute to its overall dc power transfer capability. In addition, the flexibility to interconnect HVDC networks of similar voltages, as well as the capability for bidirectional fault blocking akin to a dc circuit breaker, make the proposed DC-MMC an attractive device for deployment in future dc grids.

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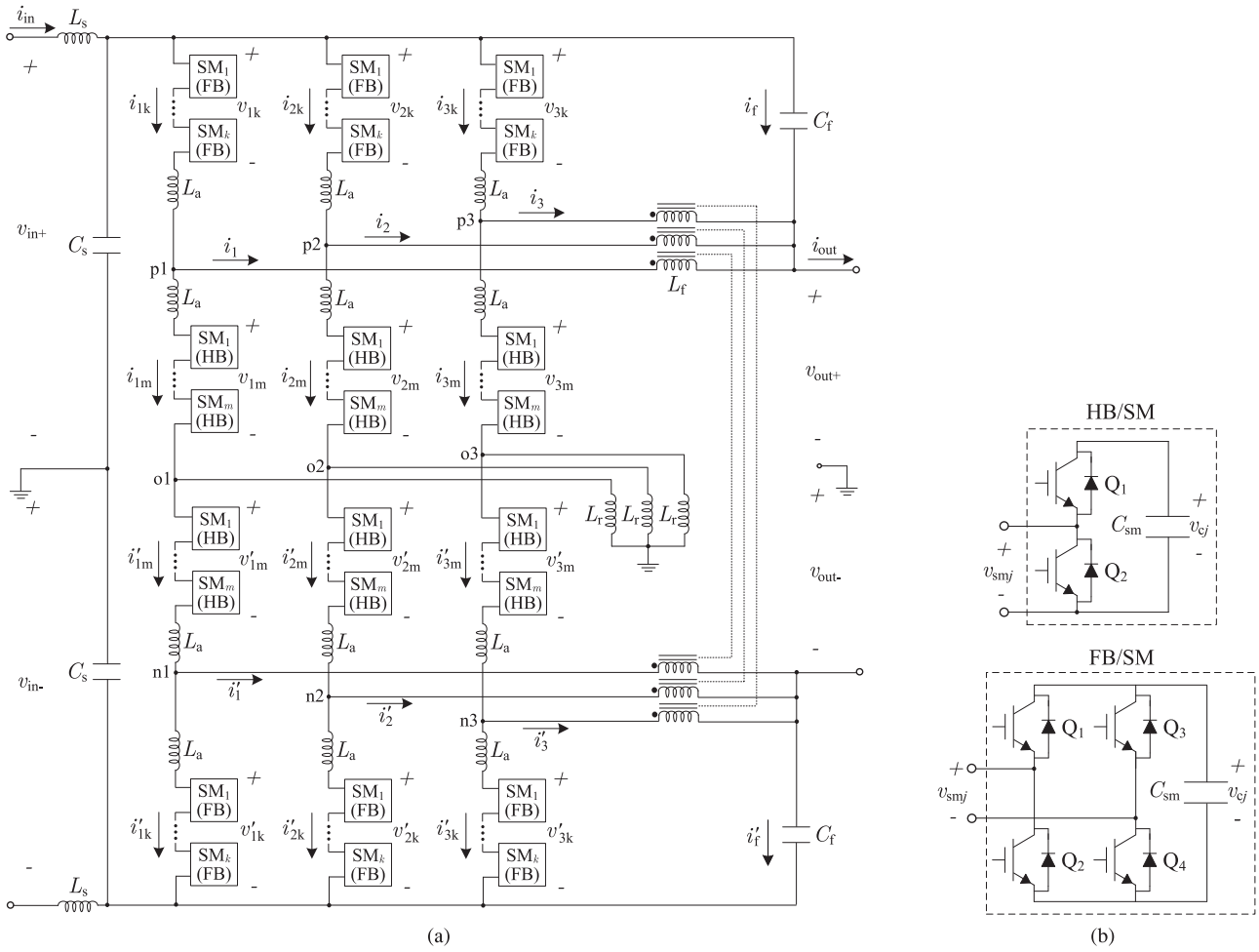

Fig. 1. Three-string DC-MMC architecture with input and output filtering: (a) circuit diagram (b) switching cell configurations for j th half-bridge SM (HB/SM) and j th full-bridge SM (FB/SM).

II. Proposed DC-MMC for HVDC Interconnects

A. Three-String Architecture

Fig. 1(a) shows the three-string architecture of the DC-MMC for deployment in bipolar HVDC networks. The DC-MMC performs single-stage dc/dc conversion by utilizing interleaved strings of cascaded SMs. Each string is comprised of two pairs of arms; each pair of arms consisting of an inner arm and an outer arm, where an arm is defined as a set of cascaded SMs. The arms of each string are series-stacked in symmetric relation about an associated midpoint, i.e., o1, o2, o3, with the inner arms flanked by the outer arms. Each inner arm and outer arm employs m half-bridge SMs (HB/SMs) and k full-bridge SMs (FB/SMs), respectively. Circuit configurations for the HB/SM and FB/SM switching cells are given in Fig. 1(b). Arm chokes $L_{\rm a}$ accommodate the switching action of the SMs. A path, enabled here by inductor $L_{\rm r}$, links the strings together via their midpoints and serves to establish circulating ac currents required by the dc/dc conversion process.

Input filtering for the DC-MMC is optionally provided by $L_{\rm s}$ and $C_{\rm s}$. However, output filter element $L_{\rm f}$ is necessary to attenuate ac voltages present at the dc output nodes of each string. The magnetizing inductance $L_{\rm f}$ of each set of coupled inductors is suitable to provide the large impedance needed for attenuation of the ac output filter currents. Moreover, use of coupled inductors as shown ensures cancellation of dc flux within the core. Capacitors $C_{\rm f}$ are a practical consideration to sink high-frequency ac currents introduced by switching action of the SMs. The use of passive elements $L_{\rm f}$ and $C_{\rm f}$ is a relatively low cost and simple implementation as compared to alternative active-filtering solutions. General sizing considerations for the output filters is provided in the Appendix.

In comparison to the three-phase dc/ac MMC, the three-string architecture in Fig. 1 shares a similar modular structure. As will become more apparent in subsequent sections, the three-string implementation of the proposed DC-MMC may be viewed as the three-phase dc/ac MMC structure adapted for single-stage dc/dc conversion. Unlike the recently proposed dc/dc converter in [37], which is formed by series-stacking two conventional three-phase dc/ac MMCs, the operation and control of Fig. 1 is fundamentally different from that of the dc/ac MMC.

B. Two-String Architecture

The DC-MMC in Fig. 1 utilizes three interleaved strings of cascaded SMs. By removing one of the strings, a two-string

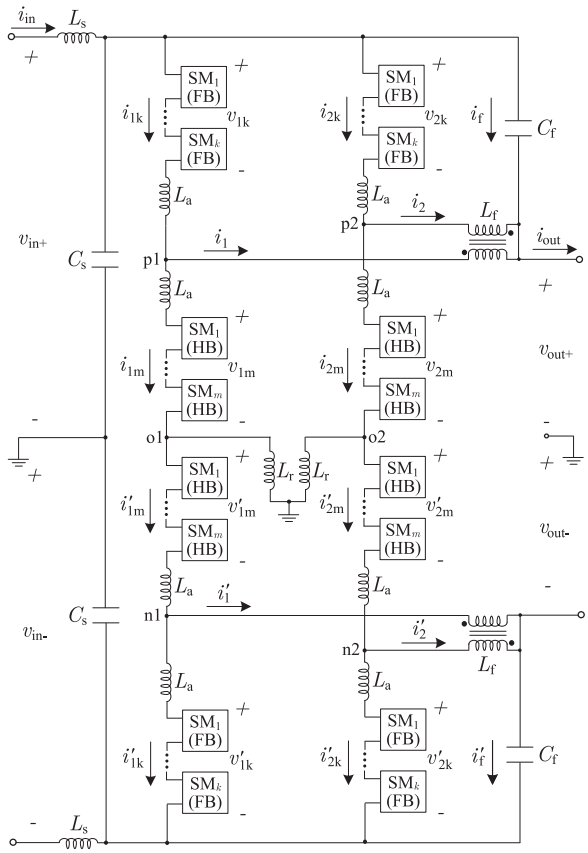

Fig. 2. Two-string DC-MMC architecture with input and output filtering.

implementation is also possible as shown in Fig. 2. This architecture is the simplest multistring implementation of the DC-MMC. In general, an arbitrary number of strings can be interleaved. Note the ability to install a coupled inductor set at each dc output pole has been exploited due to the even number of interleaved strings. Consequently, this reduces insulation requirements on the output filter inductances as compared to Fig. 1. The two-string and three-string architectures have the same fundamental principle of operation as each string employs an identical dc/dc conversion process. For equal string designs, the two-string has 2/3 the output power rating of the three-string.

C. Principle of Operation

In Figs. 1 and 2, the input network voltages $v_{\rm in+}$ and $v_{\rm in-}$ can be unevenly split between the arms of each string. For example, arm voltages $v_{1\rm k}$ (outer arm) and $v_{1\rm m}$ (inner arm) can have unequal dc components that sum to $v_{\rm in+}$. The same applies to $v'_{1\rm m}$ (inner arm) and $v'_{1\rm k}$ (outer arm) with $v_{\rm in-}$. Division of $v_{\rm in+}$ and $v_{\rm in-}$ as described is achieved by controlling the number and polarity of SM capacitors inserted along each string via switching action, where possible switching states for the jth HB/SM and FB/SM are $v_{{\rm sm}j} = \{0, +v_{{\rm c}j}\}$ and $v_{{\rm sm}j} = \{0, -v_{{\rm c}j}, +v_{{\rm c}j}\}$, respectively. The output network, represented by $v_{\rm out+}$ and $v_{\rm out-}$, is coupled across the inner arms of each string as shown. DC power transfer between networks can be reversed by changing polarity of $i_{\rm in}$. Bidirectional dc power transfer is easily accommodated as the SMs inherently permit bidirectional current flow.

The arrangement of HB/SMs and FB/SMs in Figs. 1 and 2 permits both step-up and step-down voltage level conversion for the DC-MMC. The voltage conversion ratio D and its complement D' are defined as

$$D \triangleq \frac{v_{\rm out+}}{v_{\rm in+}} = \frac{v_{\rm out-}}{v_{\rm in-}} \tag{1}$$

$$D' \triangleq 1 - D. \tag{2}$$

From (1) and (2) the operating modes of the DC-MMC are summarized:

1) step-down operation: $0 < D < 1$ and thus $0 < D' < 1$;
2) step-up operation: $D > 1$ and thus $D' < 0$.

For step-down operation where the voltages at nodes p1, p2, p3 (and n1, n2, n3) relative to ground always remain below $v_{\rm in+}$ (and above $-v_{\rm in-}$), the FB/SMs in Fig. 1 and Fig. 2 need only function as HB/SMs. That is, the FB/SMs can be replaced with HB/SMs[1] as long as the outer arms of each string are never required to inject negative voltages. However, by exploiting the additional switching state (i.e., $v_{{\rm sm}j} = -v_{{\rm c}j}$) provided by FB/SMs, the aforementioned node voltages can exceed their respective dc input rails. This enables step-up operation and thereby the ability of the DC-MMC to interconnect HVDC networks of similar voltage levels. The range of permissible voltage conversion ratios depends primarily on the SM ratio k to m and maximum allowable SM capacitor voltage. Thus, $v_{\rm out+}$ and $v_{\rm out-}$ can be generated within a range of step-up and step-down voltage conversion ratios, without the use of an intermediate ac transformer.

Step-up capability for the DC-MMC is in practice most beneficial for values of D near unity. Designing for larger values of D, e.g., $D = 1.5$, is not cost effective as the input and output terminals of the DC-MMC could in this case simply be "swapped" and the voltage conversion ratio changed accordingly, e.g., $D = 1/1.5$. However, by designing for a small step-up range around unity, for example, $0.9 < D < 1.1$, the DC-MMC can accommodate both networks fluctuating around their nominal values. This would otherwise be impossible to achieve using only HB/SMs. The DC-MMC's ability to interconnect HDVC networks of similar voltage levels is a significant operational advantage, as future HVDC grids will likely be formed in part by meshing together smaller preexisting dc grid segments—some of which will assuredly be at similar voltage levels.

The DC-MMC in Figs. 1 and 2 is able to perform single-stage dc/dc conversion by using circulating ac currents to ensure power balance for each SM capacitor. The circulating currents are established by reactive elements and serve to exchange average ac power between each outer arm and the adjacent inner arm, in a near lossless manner. To setup the circulating ac currents, the ac components of the arm voltages are synthesized such that each pair of arms generates a net ac voltage. Utilizing inductor $L_{\rm r}$ permits an optional low impedance ground reference at the converter midpoint as shown. It is also possible to

[1]Bidirectional fault blocking for the DC-MMC, which necessitates the use of FB/SMs as shown in Figs. 1 and 2, is discussed in Section IV.

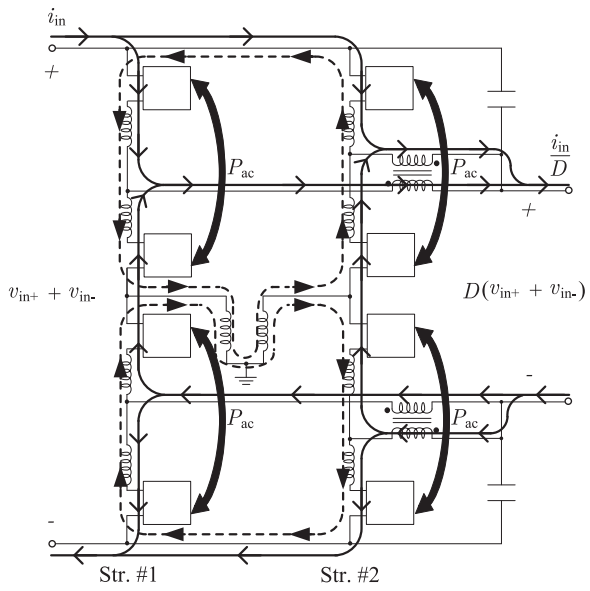

Fig. 3. Principle of operation for two-string DC-MMC architecture in Fig. 2: DC current (solid lines) and circulating ac current (dotted lines) paths are shown. Average ac power exchange between arms ($P_{\rm ac}$) for SM capacitor charge balancing is indicated by the bold arrows.

link the string midpoints using capacitors, however, this is done at the expense of high-impedance (capacitively) grounding the DC-MMC structure.

Based on the above discussion, the principle of operation of the two-string DC-MMC architecture is conceptualized in Fig. 3. As the two-string and three-string architectures have the same operating principle, the former is chosen here for simplicity. DC current paths are shown with solid lines while circulating ac current paths are represented using dotted lines. $P_{\rm ac}$ signifies the average ac power exchanged between each pair of arms for SM capacitor power balancing. A nonzero dc power transfer (i.e., $i_{\rm in} \neq 0$) necessitates a nonzero $P_{\rm ac}$ to keep the SM capacitor voltages balanced. The polarity of ac power exchange between arms depends on the DC-MMC operating mode. Although this balancing process will be analyzed later, a simple visual indicator of its necessity is that the dc current carried by each outer arm relative to the adjacent inner arm are of opposite directions. The requisite $P_{\rm ac}$ is achieved through the interaction of the circulating ac currents and ac components of the arms voltages. The shuttling of average ac power between arms is done in a near lossless manner as the circuit impedance consists of reactive elements. This power transfer mechanism, a well-known concept in traditional ac power systems for transferring average power between networks, is the key enabling mechanism by which single-stage dc/dc conversion for series-cascaded SMs is realized.

An important characteristic of the topology in Fig. 3, which also applies for Fig. 1, is the inherent symmetry in ac current paths about the converter midpoint. This symmetry, enabled by the physical linking of string midpoints, is exploited to achieve natural cancellation of ac voltages across the input and output dc terminals.

III. Analysis of DC-MMC Operation

Section II-C introduced the bipolar DC-MMC architecture and provided an overview of its principle of operation. This section discusses the DC-MMC operation in greater depth, by utilizing a simplified string model to study the ideal single-stage dc/dc conversion process. Based on the analysis, a modulation scheme for the ac arms voltages that satisfies SM capacitor power balance for all possible operating modes is proposed.

Unless otherwise indicated, the following assumptions are enforced: 1) each arm has a large number of SMs such that ideal sinusoidal ac voltages are synthesized; 2) ac voltages and currents are represented by their steady-state fundamental frequency components; 3) resistance terms are neglected; and 4) ac output filter currents are negligible. The last assumption implies $L_{\rm f}$ is sufficiently high such that, for each string, the ac filter currents are small relative to the ac component of the arms currents, e.g., $|\tilde{i}_1| \ll |\tilde{i}_{1\rm k}|, |\tilde{i}_{1\rm m}|$ and $|\tilde{i}'_1| \ll |\tilde{i}'_{1\rm k}|, |\tilde{i}'_{1\rm m}|$. The notation $\tilde{i}$ denotes the fundamental frequency component of i, i.e., $\tilde{i}(t) = \hat{I}\cos(w_{\rm m}t + \theta_{\rm i})$.

A. Single-Stage DC/DC Conversion Process

In Figs. 1 and 2, each arm of the DC-MMC can be viewed as a controllable ac voltage source with a variable dc component. However, the fundamental operating frequency of the arms voltages is not restricted to conventional 50/60 Hz. Modulating frequencies greater than 50/60 Hz can be used to reduce the size of circuit reactive components as well as the SM storage capacitors. In contrast to the MMC utilized for directly interfacing dc sources to the ac grid, the modulating frequency of the ac quantities in Figs. 1 and 2 is a selectable parameter. This design flexibility is a salient feature of the DC-MMC. Depending on the specific application, a suitable modulating frequency would be selected based on a tradeoff between design constraints such as SM capacitor voltage ripple, total energy storage cost, and switching losses.

To illustrate the ideal single-stage dc/dc conversion process, Fig. 4 provides a simplified model for string #1 of the DC-MMC. This model is valid for both Figs. 1 and 2; an identical model is obtained for the remaining string(s) by changing the appropriate variable subscripts. Observe the string model aligns with the circuit diagram in Fig. 3. This model captures all of the power transfer mechanisms involved in the energy conversion process of the DC-MMC. The cascaded SMs within each arm are represented with ideal voltage sources, which is common practice in dc/ac MMC analysis [30], [38]–[40]. These sources model both the dc and fundamental frequency ac components of the arms voltages. All currents are separated into their dc and ac parts with n denoting the number of interleaved strings, e.g., $n = 2$ for Fig. 2.

Observe from Fig. 4, the dc current through the inner arms increases as D becomes smaller. For $D < 0.5$, the inner arms carry a dc current greater than $|i_{\rm in}/n|$. This operating region thus incites high conduction losses, and may necessitate additional inner arms installed in parallel to avoid derating of power transfer between networks. The ability to parallel multiple arms is enabled by the inclusion of $L_{\rm a}$ in each arm. Restructuring

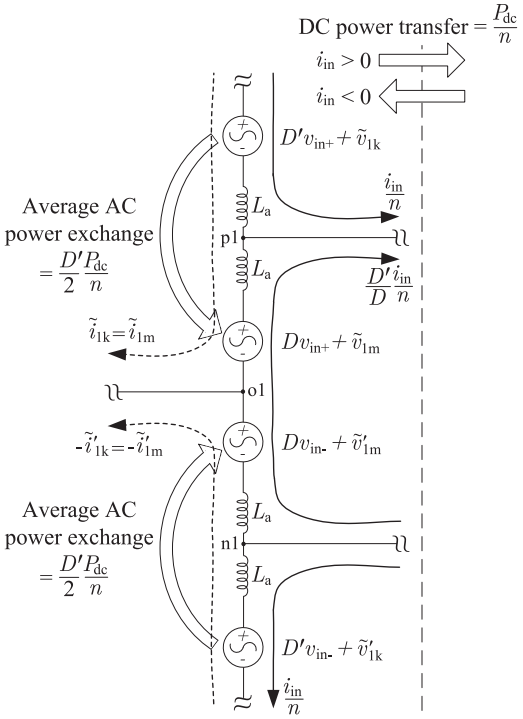

Fig. 4. Simplified model for string #1 of DC-MMC in Figs. 1 and 2, with ideal output filtering and ac filter currents neglected.

of arm chokes in Figs. 1 and 2 to eliminate individual chokes is possible, provided the basic requirement of an inductance in every voltage loop is not violated.

Each string follows the dc/dc conversion process in Fig. 4. The outer arms and inner arms of each string carry a dc current of $|i_{\rm in}/n|$ and $|(D'/D)i_{\rm in}/n|$, respectively. To ensure steady-state power balance of each SM capacitor in string #1, the following average power constraints must be met:

$$\mathbf{V}_{1\rm k} \cdot \mathbf{I}_{1\rm k} = -D'(v_{\rm in+})\frac{i_{\rm in}}{n} = -\frac{D'P_{\rm dc}}{2n} \tag{3}$$

$$\mathbf{V}_{1\rm m} \cdot \mathbf{I}_{1\rm m} = D'(v_{\rm in+})\frac{i_{\rm in}}{n} = \frac{D'P_{\rm dc}}{2n} \tag{4}$$

$$\mathbf{V}'_{1\rm m} \cdot \mathbf{I}'_{1\rm m} = D'(v_{\rm in-})\frac{i_{\rm in}}{n} = \frac{D'P_{\rm dc}}{2n} \tag{5}$$

$$\mathbf{V}'_{1\rm k} \cdot \mathbf{I}'_{1\rm k} = -D'(v_{\rm in-})\frac{i_{\rm in}}{n} = -\frac{D'P_{\rm dc}}{2n}. \tag{6}$$

$\mathbf{V}_{1\rm k} \cdot \mathbf{I}_{1\rm k}$ denotes the phasor dot product, i.e., $\mathbf{V}_{1\rm k} \cdot \mathbf{I}_{1\rm k} = (\hat{V}\hat{I}/2)\cos(\theta_{\rm v} - \theta_{\rm i})$. The notation $\mathbf{V}_{1\rm k}$ and $\mathbf{I}_{1\rm k}$ signifies the fundamental frequency ac rms phasors for $\tilde{v}_{1\rm k}$ and $\tilde{i}_{1\rm k}$, respectively. That is, $\mathbf{V}_{1\rm k} = (\hat{V}/\sqrt{2})\angle\theta_{\rm v}$ and $\mathbf{I}_{1\rm k} = (\hat{I}/\sqrt{2})\angle\theta_{\rm i}$. $P_{\rm dc}$ is the total dc power transfer between networks, as shown in Fig. 4, where $P_{\rm dc} > 0$ corresponds to $i_{\rm in} > 0$.

Power balance constraints (3) through (6) reveal an average ac power equal to $|D'P_{\rm dc}/2n|$ must be exchanged between each outer arm and the adjacent inner arm. This is the same power exchange as given by $P_{\rm ac}$ in Fig. 3, however, in Fig. 4 the polarity is explicitly shown. The direction of power exchange depends on the polarities of D' (step-up/step-down) and $P_{\rm dc}$ (dc power transfer direction). For example, Fig. 4 shows the outer arms must deliver average ac power to the inner arms for: 1) $D' > 0,\ P_{\rm dc} > 0$; and 2) $D' < 0,\ P_{\rm dc} < 0$.

A set of constraints similar to (3) through (6) can be formulated for the remaining string(s) in Figs. 1 and 2. To ensure a net ac voltage is not impressed across the input or output dc terminals, requirements are imposed on the synthesized arms voltages

$$\mathbf{V}_{1\rm k} = -\mathbf{V}'_{1\rm k} \tag{7}$$

$$\mathbf{V}_{1\rm m} = -\mathbf{V}'_{1\rm m}. \tag{8}$$

In general, symmetry constraints similar to (7) and (8) are imposed on each string. Taking into consideration the phase shift between modulating waveforms of each string, interleaving of strings as shown in Figs. 1 and 2 offers natural cancellation of ac output inductor currents independent of D. For example, $\tilde{i}_1$ and $\tilde{i}_2$ in Fig. 2 always sum to zero as they are phase shifted by 180°. As a result, $C_{\rm f}$ ideally carries zero current and pole voltages $v_{\rm out+}$ and $v_{\rm out-}$ are free of fundamental frequency ac stimuli. However, in practice $C_{\rm f}$ will carry a small amount of high-frequency current due to switching of the SMs.

Based on the preceding discussion, the DC-MMCs in Figs. 1 and 2 internally circulate a total average ac power of $|D'P_{\rm dc}|$. Note interconnecting two HVDC networks of similar voltage levels requires only a small amount of ac power to be circulated. In contrast, for $D = 0.5$ the DC-MMC must internally circulate 50% of the total dc power transfer in terms of ac power.

B. Steady-State Power Balance of SM Capacitors

There are infinitely many combinations of ac arms voltages and resulting ac arms currents that can satisfy power balance constraints (3) through (6) and arms voltage constraints (7) and (8). The same notion applies to a similar set of equations that can be formulated for the remaining string(s) in Figs. 1 and 2. However, only the two-string architecture is analyzed in this section as it is the simplest multistring implementation of the DC-MMC. In particular, ac phasor diagrams used in converter analysis are simplified, ensuring key aspects of the single-stage dc/dc conversion process are clearly illustrated.

Fig. 5 gives two example ac phasor diagrams that illustrate the fundamental power transfer mechanism employed to achieve steady-state power balance of each SM capacitor in Fig. 2, for all possible operating modes of the DC-MMC. The peak magnitude of the ac arms voltages is denoted by $\hat{V}$. Φ is the phase shift between ac voltages of each outer arm and the adjacent inner arm, with positive values of Φ defined for the inner arm voltage leading the outer arm voltage. For example, positive values of Φ for string #1 correspond to $\mathbf{V}_{1\rm m}$ leading $\mathbf{V}_{1\rm k}$ and $\mathbf{V}'_{1\rm m}$ leading $\mathbf{V}'_{1\rm k}$. Note the modulating waveforms of each string are displaced by 180°.

It is easy to visualize via phasor dot products that each pair of inner and outer arms in Fig. 5 exchange equal average ac power as dictated by (3) through (6). However, adopting such a strategy constrains each pair of arms to equally share the reactive power requirements of the composite load formed by $L_{\rm r}$ and $L_{\rm a}$. This implies each arm operates at an equal ac power factor (in Fig. 5, the example case of power factor equal to 0.707

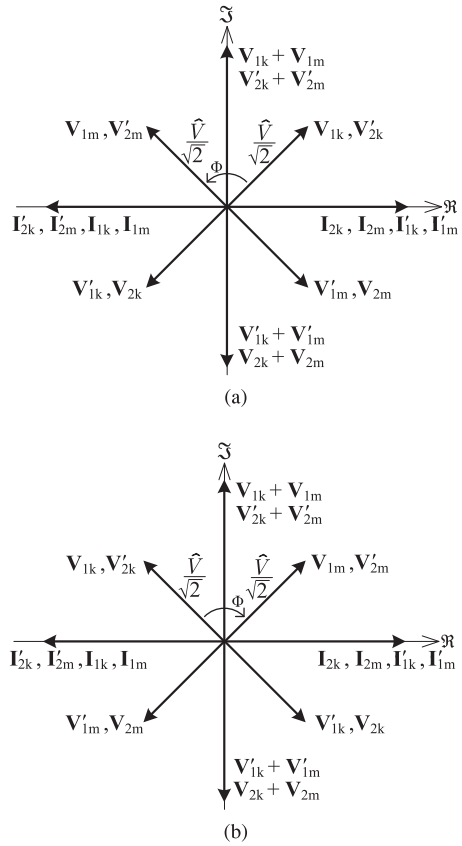

Fig. 5. Fundamental frequency ac rms phasor diagrams that illustrate the power transfer mechanism used to achieve power balance of SM capacitors in Fig. 2, with ac output filter currents neglected, valid for: (a) $D<1,\ i_{\rm in}>0$ and $D>1,\ i_{\rm in}<0$; (b) $D<1,\ i_{\rm in}<0$ and $D>1,\ i_{\rm in}>0$.

is shown where $\Phi=\pm 90^{\circ}$). A preferred strategy is to impose unity power factor on the outer arms while realizing near unity power factor operation for the inner arms as shown in Fig. 6. Here, M is the ratio of inner arm to outer arm ac voltage magnitudes, e.g., $M=|\mathbf{V}_{1\rm m}/\mathbf{V}_{1\rm k}|$. For a fixed $\hat{V}$, this modulation scheme minimizes the circulating ac currents needed for the dc/dc conversion process when operating with larger values of D (further details in Section V). Moreover, it significantly reduces the circuit reactance required to establish the circulating ac currents.

Based on Figs. 4 and 6, the average power exchanged between each outer arm and the adjacent inner arm is

$$P_{\rm k/m}=\frac{M\hat{V}^2}{4X_{\rm r}}\sin\Phi \tag{9}$$

where

$$X_{\rm r}=\omega_{\rm m}(L_{\rm r}+L_{\rm a}). \tag{10}$$

Positive values of $P_{\rm k/m}$ denote average ac power delivered from each outer arm to the adjacent inner arm of the same string. In general, $P_{\rm k/m}$ is adjusted by changing any combination of M, $\hat{V}$ or Φ. Converters designed with smaller $X_{\rm r}$ offer reduced circuit var requirements and result in values of $|\Phi|$ approaching 180°.

Equation (10) reveals the DC-MMC can in fact be operated with $L_{\rm r}$ equal to zero. That is, the midpoints of each string in

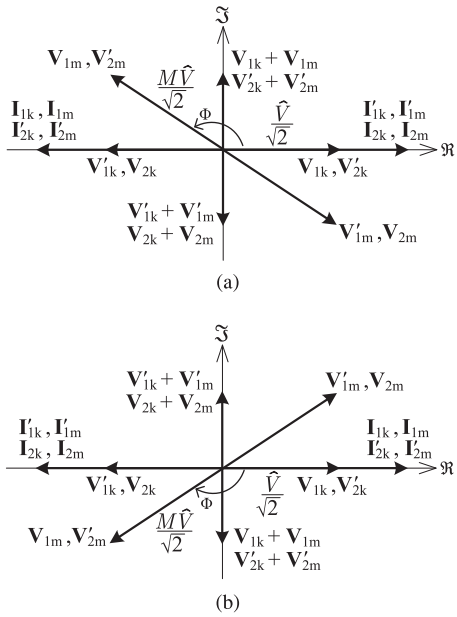

Fig. 6. Fundamental frequency ac rms phasor diagrams depicting modulation strategy to ensure power balance of SM capacitors in Fig. 2 while imposing unity power factor on outer arms and near unity power factor operation on inner arms, with ac output filter currents neglected, valid for: (a) $D<1,\ i_{\rm in}>0$ and $D>1,\ i_{\rm in}<0$; (b) $D<1,\ i_{\rm in}<0$ and $D>1,\ i_{\rm in}>0$.

Fig. 2 (and similarly Fig. 1) can be connected together and, possibly, or, if desired, solidly grounded. In this case, the arm chokes solely provide the reactance needed to setup the circulating ac currents. However, it must be stressed midpoint inductors $L_{\rm r}$ need only to carry ac currents while arm chokes $L_{\rm a}$ must carry both dc and ac currents. Allocation of circuit inductance to $L_{\rm r}$ versus $L_{\rm a}$ is the outcome of a converter design optimization, which therefore enables cost reduction and is outside the scope of this paper. The simulations in Section V utilize a nonzero $L_{\rm r}$.

Equating (9) with the required average power exchange as dictated by (3) through (6) gives

$$\frac{M\hat{V}^2}{4X_{\rm r}}\sin\Phi=\frac{D'P_{\rm dc}}{2n}. \tag{11}$$

Power balance criteria (11) is a primary design equation quantifying the amount of average ac power that must be exchanged between arms in steady state, as a function of the voltage conversion ratio and dc power transfer between HVDC networks. Furthermore, (11) provides additional insight into DC-MMC operation as it relates ac and dc power transfer mechanisms. Substituting $n=2$ reveals each pair of arms in Fig. 2 exchange $|D'P_{\rm dc}/4|$ of average ac power via circulating ac currents.

IV. Bidirectional DC Fault Blocking Capability

In addition to enabling step-up operation and the interconnection of HVDC networks with similar voltage levels, the FB/SMs in Figs. 1 and 2 can provide bidirectional fault blocking. That is, the DC-MMC can interrupt fault currents initiated by dc faults in either the input or output side networks similar to a dc circuit breaker. This is accomplished by controlling the FB/SMs in Figs. 1 and 2 to impose the appropriate polarity of voltage

TABLE I
DC-MMC BIDIRECTIONAL FAULT BLOCKING CAPABILITY: OUTER ARMS SM BLOCKING VOLTAGE REQUIREMENTS

Outer Arms SM Blocking Voltage Requirements (Normalized Relative to $v_{\mathrm{in}+} + v_{\mathrm{in}-}$)		
Fault Condition	**Step-Down Operation** ($D < 1$)	**Step-Up Operation** ($D > 1$)
Input Side Network Fault (Block Output Network Voltage)	D [p.u.] (FB/SMs) (Inject Negative Voltage)	D [p.u.] (FB/SMs) (Inject Negative Voltage)
Output Side Network Fault (Block Input Network Voltage)	1.0 [p.u.] (HB/SMs) (Inject Positive Voltage)	1.0 [p.u.] (HB/SMs) (Inject Positive Voltage)
Bidirectional Fault Blocking Capability	D [p.u.] (FB/SMs) + D' [p.u.] (HB/SMs) (Inject Pos./Neg. Voltages)	D [p.u.] (FB/SMs) (Inject Pos./Neg Voltages)
Example Scenario	**Step-Down Operation** ($D < 1$)	**Step-Up Operation** ($D > 1$)
$D = 0.5$	0.5 [p.u.] (FB/SMs) + 0.5 [p.u.] (HB/SMs) = 1.0 [p.u.]	———
$D = 0.8$	0.8 [p.u.] (FB/SMs) + 0.2 [p.u.] (HB/SMs) = 1.0 [p.u.]	———
$D = 1.1$	———	1.1 [p.u.] (FB/SMs)

during fault events, thereby blocking the flow of fault currents. This strategy is similar to the recognized fault blocking scheme for the dc/ac MMC [10], [41]. The inner arms of the DC-MMC need only to employ HB/SMs as no benefit is realized with bipolar voltage injection. In general, to ensure bidirectional fault blocking the $2k$ outer arm SMs within each string must collectively provide enough blocking voltage to counteract the larger of $v_{\mathrm{in}+} + v_{\mathrm{in}-}$ and $v_{\mathrm{out}+} + v_{\mathrm{out}-}$.

Table I summarizes the fault blocking capability of the DC-MMC. The blocking voltages required for the outer arms are provided in p.u. (normalized relative to input side dc network voltage) and are partitioned into individual HB/SM and FB/SM requirements. For example, a value of "0.6 p.u. (FB/SMs)" signifies that the outer arms of each string must have enough FB/SMs to support 60% of the input network voltage.

Table I illustrates that faults located in the input side network require the outer arms to inject a negative voltage to counteract the output side network. This necessitates the use of FB/SMs. The amount of p.u. negative voltage to be injected is equal to the voltage conversion ratio D, and is the same for both step-down and step-up modes. In the case of faults located in the output side network, the outer arms must inject a positive voltage to counteract the input side network. HB/SMs are sufficient to provide the 1.0 p.u. positive voltage injection for both step-down and step-up modes. To achieve bidirectional fault blocking for step-down operation, only D p.u. of FB/SMs are needed (where $D < 1$) to block both input and output side faults. To minimize the total semiconductor cost HB/SMs are used for the remaining D' p.u. of blocking voltage (i.e., $D + D' = 1.0$). During step-up operation, D p.u. of FB/SMs are necessary (where $D > 1$).

V. OPEN LOOP VOLTAGE CONTROL AND SIMULATION RESULTS

Open loop control techniques for balancing of SM capacitor voltages within the dc/ac MMC have been discussed in several papers [38], [42]–[46]. One of the simplest forms of open loop control, direct modulation [38] adopts fixed sinusoidal modulating signals for the MMC arms. Balancing of SM capacitor voltages is achieved by a sort and selection algorithm that arranges capacitors based on their voltage measurements, and inserts the appropriate one(s) at each switching instant based on arm current measurements. This basic modulation scheme, although allowing second harmonic currents to circulate between phase legs [38], is sufficient to maintain stable power transfer between dc and ac side terminals of the dc/ac MMC. However, such a modulation approach alone is inherently incapable of maintaining voltage balance of SM capacitors for the DC-MMC. This is because the DC-MMC employs a fundamentally different power transfer mechanism: the direct exchange of average ac power between arms (see Fig. 4). Any slight imbalance in this power exchange will cause the SM capacitor voltages to diverge. Consequently, some form of regulation is required.

Section V-A proposes a closed loop ac current control strategy that ensures balancing of the SM capacitor voltages by regulating the average ac power exchanged between inner and outer arms. This enables open loop voltage control of the DC-MCC.

A. Circulating AC Current Control

Fig. 7 shows the proposed circulating ac current control scheme that enables open loop voltage control of the two-string DC-MMC. The control structure is partitioned into four blocks for each string; inner and outer arm logic for the positive and negative poles. To maintain power balance of the SM capacitors, closed loop control of the circulating ac currents is adopted according to the modulation strategy in Fig. 6. As previously described the outer arms are imposed to operate at unity power factor while the inner arms operate at near unity power factor. This choice is based on the principle that, for larger D, the outer arms will likely have less available voltage headroom (as $|D'| \ll 0.5$) and therefore their ac voltage should be maximized. However, the inner arms can alternatively operate at unity power factor by simply mirroring the inner/outer arms logic in Fig. 7. In general, the proposed control can be modified to split the vars generation between arms as desired.

In Fig. 7, the ac component of the outer arms modulating signals are fixed for each string. In contrast, the ac component of the inner arms modulating signals are the outcome of closed-loop control action. Proportional-resonant compensators synthesize the inner arms ac voltages needed to drive the circulating ac currents in phase with the outer arms. AC current references for the outer arms are generated by proportional-integral (PI) compensators acting on the error between the sum of inner arm minus outer arm SM capacitor voltages. When this error deviates from zero, which signifies an imbalance in the ac power exchange between arms, the PI compensators adjust the magnitude of circulating ac currents to reestablish SM capacitor power balance. High-pass filters used in the feedback loop ensure the compensators to act only on the ac component of the outer arms

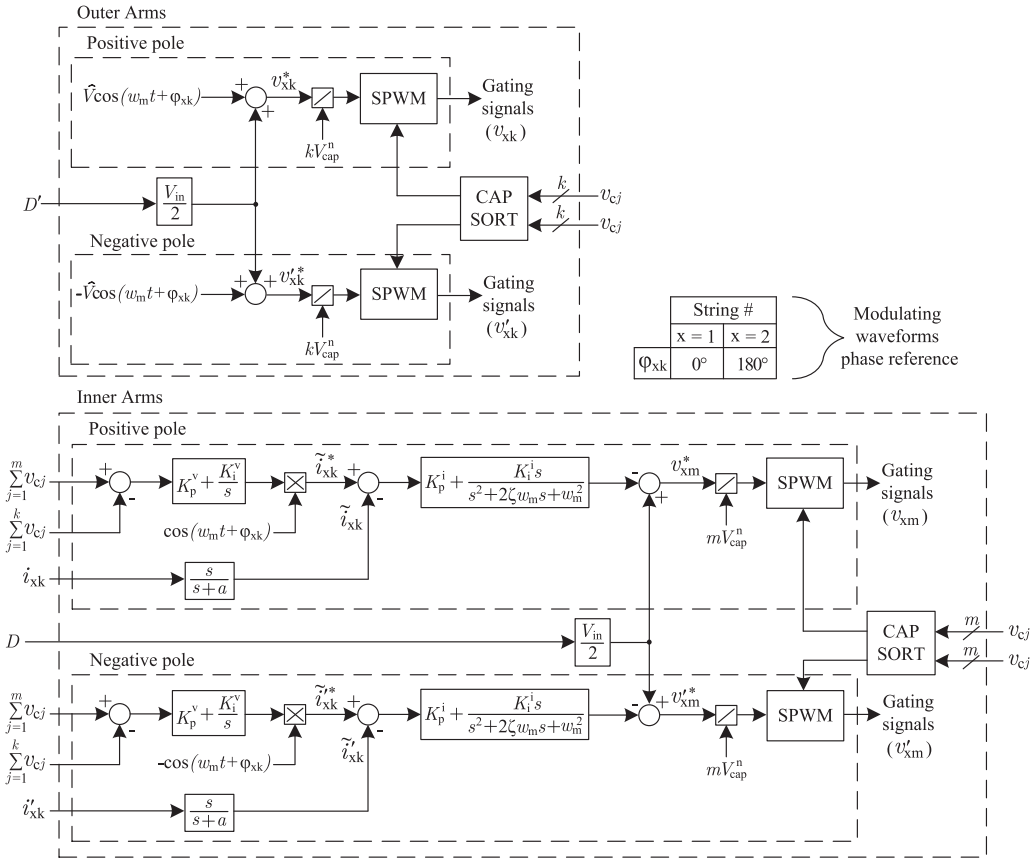

Fig. 7. Circulating ac current control for each string (i.e., x $\in \{1, 2\}$) enabling open loop voltage control of the two-string DC-MMC.

currents. Similar to the dc/ac MMC, a sort algorithm [47] orders the SM capacitors in each arm from lowest to highest voltages. Using the reference voltage modulating signals for each arm, e.g., $[v_{1\mathrm{k}}^{*}, v_{1\mathrm{m}}^{*}, v_{1\mathrm{m}}^{\prime *}, v_{1\mathrm{k}}^{\prime *}]$ for string #1, the SPWM blocks generate gating signals by selecting the appropriate SM capacitor(s) (via sort algorithm) to insert at each switching instant based on arm current direction and arm voltage polarity. The nominal voltage of each SM capacitor is denoted by $V_{\mathrm{cap}}^{\mathrm{n}}$.

In Fig. 7, the dc components of the modulating signals are fixed for all arms based on the desired converter voltage conversion ratio D. This is sufficient for open loop voltage control of the DC-MMC. In practice, additional control loop(s) would be needed to regulate the dc output currents from each string to ensure proper current/power sharing between strings.

TABLE II
PLECS SIMULATION PARAMETERS FOR FIG. 2 ($k = m = 4$)

Converter Parameters	**Value**
DC input network voltage, $v_{\mathrm{in}+} + v_{\mathrm{in}-}$	17.6 kV
Arm choke, L_{a}	2.5 mH
Midpoint string inductor, L_{r}	0.5 mH
SM capacitor, C_{sm}	20 mF
Output filter rms winding voltage, $(V_{\mathrm{f}}^{\max})_{\mathrm{rms}}$	2.47 kV
Output filter rms winding current, $(I_{\mathrm{f}}^{\max})_{\mathrm{rms}}$	0.795 kA
Output filter magnetizing inductance, L_{f}	990 mH
Output filter capacitor, C_{f}	15 μF
Fundamental modulating frequency, f_{m}	50 Hz
Carrier frequency, f_{c}	2.5 kHz
Control Parameters	**Value**
Proportional gain, $K_{\mathrm{p}}^{\mathrm{v}}$	0.1 A/V
Proportional gain, $K_{\mathrm{p}}^{\mathrm{i}}$	2 V/A
Integral gain, $K_{\mathrm{i}}^{\mathrm{v}}$	8 A/Vs
Resonant gain, $K_{\mathrm{i}}^{\mathrm{i}}$	600 V/As
Resonant damping term, ζ	0.01
High-pass filter pole, a	15 rad/s

B. PLECS Simulation Results

Two operating scenarios for the two-string DC-MMC are simulated in PLECS to validate the open-loop voltage control strategy proposed in Fig. 7. The scenarios include: 1) $D = 0.5$ (step-down); and 2) $D = 1.1$ (step-up). For each scenario, the dc power transfer between networks P_{dc} is 14 MW. A full switched model of Fig. 2 is implemented with four SMs per arm, i.e., $k = m = 4$; ideal switches are utilized. In both cases $i_{\mathrm{in}} > 0$ (and thus $P_{\mathrm{dc}} > 0$) such that Fig. 6(a) and (b) is utilized. To ensure power balance of SM capacitors, the two-string DC-MMC must exchange $D' P_{\mathrm{dc}}/4$ of average ac power between inner and outer arms (see Fig. 4). The fundamental modulating frequency of the arms voltages is selected as 50 Hz. The APOD SPWM scheme [47] is adopted, although alternative modulation schemes can be used. Simulation parameters are given in Table II. In the subsequent discussions, the string model in Fig. 4 and phasors diagrams in Fig. 6 are heavily leveraged in comparing simulation results with the DC-MMC analysis in Section III.

1) Step-Down Operation: Simulation results for $D = 0.5$ with dc power transfer from input to output are given in Fig. 8.

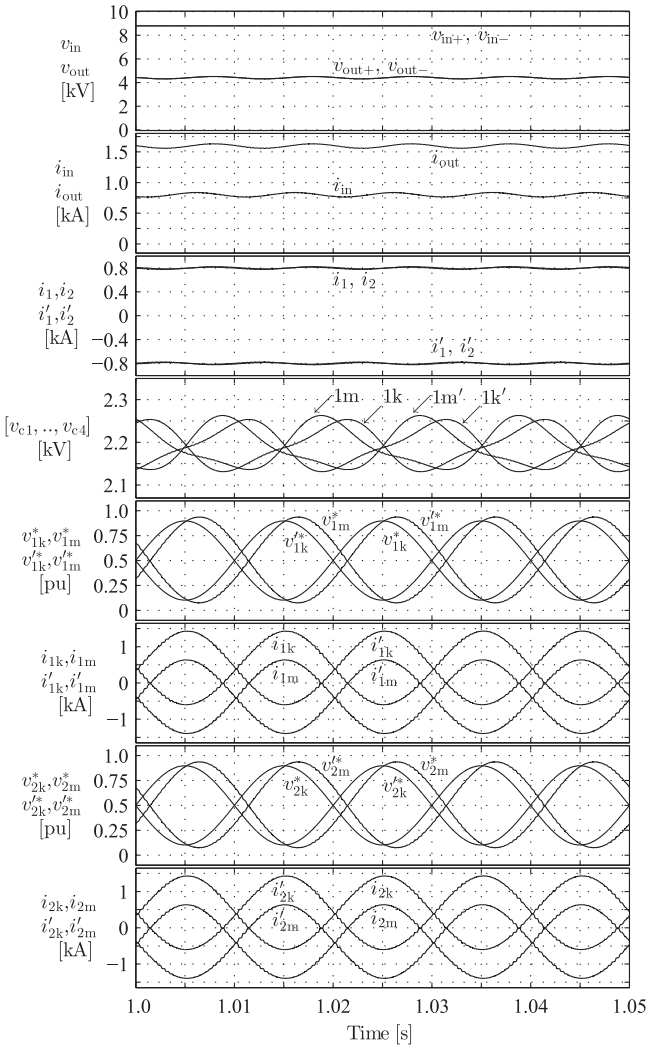

Fig. 8. Simulation results for two-string DC-MMC with $D = 0.5$ and $i_{\rm in} > 0$; $\hat{V} = 3.5\ {\rm kV_{pk}}$, $V^{\rm n}_{\rm cap} = 2.2\ {\rm kV}$, $L_{\rm s} = 0\ {\rm mH}$, $C_{\rm s} = 0\ \mu{\rm F}$.

The dc input and output voltages are ± 8.8 and ± 4.4 kV, respectively. $i_{\rm in}$ and $i_{\rm out}$ have average values of 0.795 and 1.59 kA, respectively. For the DC-MMC to facilitate the transfer of 14 MW, each outer arm delivers $D'P_{\rm dc}/4 = 1.75$ MW of average ac power to the adjacent inner arm (i.e., $P_{\rm k/m} = +1.75$ MW). This is achieved with an ac voltage for the outer arms of $\hat{V} = 3.5\ {\rm kV_{pk}}$ and circulating ac currents of $1.0\ {\rm kA_{pk}}$.

Fig. 8 shows the ac currents in the arms circulate in a symmetric fashion about the converter midpoint as dictated by Fig. 4, e.g., $\tilde{i}_{1\rm k} = \tilde{i}_{1\rm m} = -\tilde{i}'_{1\rm m} = -\tilde{i}'_{1\rm k}$. All of the arms have the same dc current magnitude of 0.398 kA ($i_{\rm in}/2$) due to the fact $D' = D = 0.5$. However, outer arms currents $i_{1\rm k}, i'_{1\rm k}, i_{2\rm k}, i'_{2\rm k}$ have a positive average value (+0.398 kA) while inner arms currents $i_{1\rm m}, i'_{1\rm m}, i_{2\rm m}, i'_{2\rm m}$ have a negative average value (–0.398 kA). The opposing polarity of dc arms currents aligns with Fig. 4 and is a result of the DC-MMC operating in step-down mode. As demonstrated by i_1, i_2 and i'_1, i'_2 waveforms, $L_{\rm f}$ imposes a large ac impedance and confines the circulating ac currents within the DC-MMC structure. This validates the prior assumption of negligible ac output inductor currents.

In Fig. 8, the ac components of the arms modulating signals (i.e., scaled versions of ac arms voltages) and ac components of the arms currents align with the phasor diagram in Fig. 6(a). Average ac power is delivered from each outer arm to the adjacent inner arm, with outer arms operating at unity power factor and inner arms supplying the necessary vars. For example, $\tilde{v}^*_{1\rm k}$ and $\tilde{i}_{1\rm k}$ in Fig. 8 are phase-shifted 180° (outer arm delivering average ac power at unity power factor) while $\tilde{v}^*_{1\rm m}$ slightly lags $\tilde{i}_{1\rm m}$ (inner arm receiving average ac power near unity power factor and supplying vars). To supply reactive power the inner arms have a slight larger ac voltage magnitude relative to the outer arms, as illustrated in Fig. 6(a). SM capacitor voltage waveforms plotted for string #1 verify charge balance is achieved via the described power transfers. Similar waveforms exist for string #2. The balancing of SM capacitor voltages as shown validates the adopted closed loop ac current control strategy.

As can be seen in Fig. 8, $i_{\rm in}$ and $i_{\rm out}$ contain a small second harmonic (i.e., 100 Hz) ripple component. This open-loop operating characteristic of the DC-MMC is not captured in Section III as the analysis is restricted to fundamental frequency operation. The second harmonic current ripple can be mitigated by increasing the energy storage capacity of the SMs (i.e., increasing $C_{\rm sm}$). Furthermore, it is likely that supplemental arm voltage control can be incorporated to suppress the generation of second harmonic voltages, similar to the dc/ac MMC [48]. For this case study, the SM capacitors are sized to achieve acceptable 100-Hz current ripple as well as tolerable capacitor voltage ripple.

2) Step-Up Operation: Simulation results for $D = 1.1$ are provided in Fig. 9. The input voltage of ± 8.8 kV is now stepped up to ± 9.68 kV. This scenario is chosen to demonstrate the DC-MMC's ability to interconnect dc networks of similar voltages by exploiting FB/SMs in the outer arms. The average value of $i_{\rm in}$ remains the same as for step-down mode (0.795 kA), however, $i_{\rm out}$ now has an average value of 0.723 kA due to the relation $i_{\rm in} = Di_{\rm out}$. For the same $P_{\rm dc} = 14$ MW, only 0.35 MW of average ac power is exchanged between arms in Fig. 9 as opposed to the 1.75 MW needed for step-down operation with $D = 0.5$. This is because $|D'|$ has decreased from 0.5 to 0.1. However, as $D' = -0.1$ but $P_{\rm dc}$ remains positive, the polarity of power exchange has reversed and is now from inner to outer arms (i.e., $P_{\rm k/m} = -0.35$ MW). This is achieved with $\hat{V} = 1.2\ {\rm kV_{pk}}$ and circulating ac currents of $0.583\ {\rm kA_{pk}}$.

The average value of outer arms currents $i_{1\rm k}, i'_{1\rm k}, i_{2\rm k}, i'_{2\rm k}$ in Fig. 9 remains unchanged from the simulated step-down scenario (+0.398 kA), which is consistent with Fig. 4. The dc component of inner arms currents $i_{1\rm m}, i'_{1\rm m}, i_{2\rm m}, i'_{2\rm m}$, however, is now +0.036 kA, i.e., flowing toward the neutral, as necessary for boost operation. Relative to the outer arms, the inner arms of the DC-MMC need only carry a small amount of dc current for values of D near unity.

In Fig. 9, the ac components of the arms modulating signals and the ac arms currents align with the phasor diagram in Fig. 6(b). Average ac power exchange is now from each inner arm to the adjacent outer arm. The outer arms still operate at

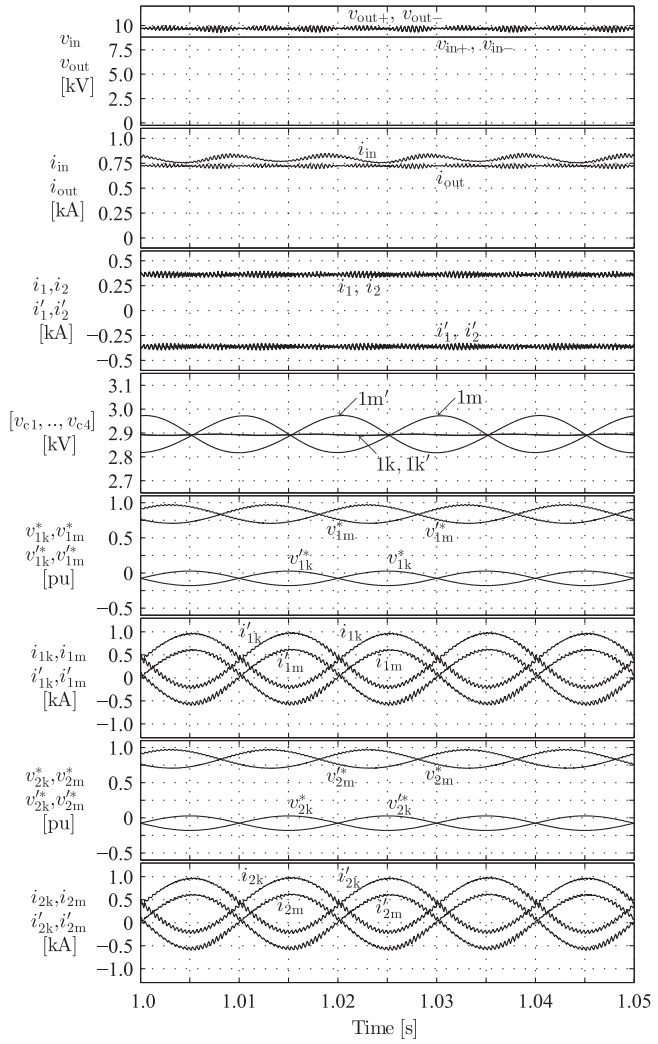

Fig. 9. Simulation results for two-string DC-MMC with $D = 1.1$ and $i_{\rm in} > 0$; $\hat{V} = 1.2\ {\rm kV_{pk}}$, $V^{\rm n}_{\rm cap} = 2.9\ {\rm kV}$, $L_{\rm s} = 0.5\ {\rm mH}$, $C_{\rm s} = 40\ \mu{\rm F}$.

unity power factor while the inner arms supply vars. For example, $\tilde{v}^*_{\rm 1k}$ and $\tilde{i}_{\rm 1k}$ in Fig. 9 are in phase (outer arm receiving average ac power at unity power factor) while $\tilde{v}^*_{\rm 1m}$ lags $\tilde{i}_{\rm 1m}$ by nearly 180° (inner arm delivering average ac power near unity power factor and supplying vars). The described waveforms demonstrate the DC-MMC's ability to meet power balance of each SM capacitor while performing step-up voltage level conversion.

To facilitate step-up operation the nominal voltage of each SM capacitor in Fig. 9 has increased from 2.2 to 2.9 kV. This increase in $V^{\rm n}_{\rm cap}$, which for simplicity in this case study is imposed for all arms, permits the inner arms to achieve the dc output voltage required for step-up mode.

In comparison to Fig. 8, the waveforms for step-up operation display significantly more switching ripple content. This stems from using a relatively low number of SMs in each arm (four) in order to reduce the simulation complexity and runtime. To compensate for the low number of SMs, the arm choke inductance and SPWM carrier frequency are selected to accommodate the added ripple during step-up. In addition, input filter elements $L_{\rm s} = 0.5$ mH and $C_{\rm s} = 40\ \mu$F are utilized for the step-up scenario to reduce switching ripple for $i_{\rm in}$. For the step-down scenario, an input filter is not required. This is affirmed by very low switching ripple content in Fig. 8. Note, in both Figs. 8 and 9 the DC-MMC can provide bidirectional fault blocking as the outer arms have sufficient voltage to withstand the larger of the input or output dc terminal voltages.

VI. Experimental Validation of Single-Stage DC/DC Conversion Process

In this section, experimental results are presented for a 4-kW laboratory prototype based on a single-string implementation of the DC-MMCs in Figs. 1 and 2. The single string is the simplest realization of the bipolar DC-MMC and operates in a fundamentally similar manner to that described for the multistring architectures. Although consisting of a single SM string, the prototype enables practical validation of the ability to satisfy power balance of SM capacitors via circulating ac currents—the key power transfer mechanism enabling single-stage dc/dc conversion for the studied multistring architectures. The main objective of the experimental work is to support the DC-MMC simulations, by demonstrating successful field implementation of the proposed energy conversion concept; notably, the circulating ac currents remain confined to the converter structure despite typical load and parameter imbalances. Such nonideal conditions are not represented in the simulations. The experiments include step-down and step-up scenarios similar to those studied in Section V.

Fig. 10 shows the circuit diagram and experimental layout for the single-string DC-MMC. The converter structure in Fig. 10(a) is obtained by replacing string #2 in Fig. 2 with two series-connected capacitors $C_{\rm r}/2$. These capacitors perform the functionality of the midpoint reactors $L_{\rm r}$ and permit the ac currents to circulate within the converter structure. Compared to the multistring architectures, the single-string lacks the following benefits: 1) a low impedance ground reference at converter midpoint; and 2) natural cancellation of ac inductor currents at the output. The model in Fig. 4 remains valid for the single-string architecture, but with (10) now defined as

$$X_{\rm r} = -(\omega_{\rm m} C_{\rm r})^{-1} + \omega_{\rm m} L_{\rm a}. \tag{12}$$

Note (12) implies the net circuit reactance can be either capacitive (<0) or inductive (>0). The converter in Fig. 10(b) is designed with $X_{\rm r} > 0$ as $L_{\rm a}$ is selected sufficiently large to limit the switching ripple that results from using a low number of SMs.

The open-loop voltage control in Fig. 7 is adopted. The control logic is implemented on a real-time Linux-based PC controller with integrated FPGA. Circuit and control parameters are given in Table III.

A. Step-Down Operation

Fig. 11 shows experimental results for step-down operation with $v_{\rm in} = 478$ V, $v_{\rm out} = 240$ V, and $P_{\rm out} = 4.0$ kW. This experiment supplements the step-down simulation in Fig. 8. To account for converter losses and switch dead-time, D is

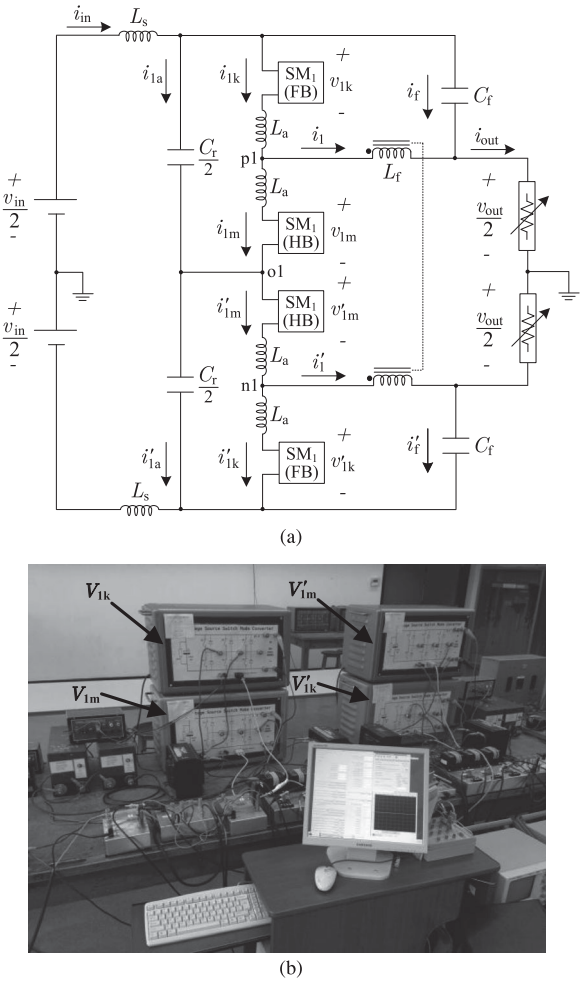

Fig. 10. Single-string implementation of DC-MMCs in Fig. 1 and Fig. 2 with $k = m = 1$ as basis for 4-kW laboratory prototype: (a) circuit diagram (b) experimental layout.

TABLE III
EXPERIMENTAL PARAMETERS FOR FIG. 10

Converter Parameters	Value
DC input network voltage, $v_{\rm in}$	480 V
Arm choke, $L_{\rm a}$	5 mH
Midpoint capacitor, $C_{\rm r}/2$	5.3 mF
SM capacitor, $C_{\rm sm}$	2.4 mF
Output filter rms winding voltage, $(V_{\rm f}^{\rm max})_{\rm rms}$	66.5 V
Output filter rms winding current, $(I_{\rm f}^{\rm max})_{\rm rms}$	16.7 A
Output filter magnetizing inductance, $L_{\rm f}$	2210 mH
Output filter capacitor, $C_{\rm f}$	10 μF
Fundamental modulating frequency, $f_{\rm m}$	50 Hz
Switching frequency, $f_{\rm sw}$	5 kHz
Control Parameters	**Value**
Proportional gain, $K_{\rm p}^{\rm v}$	0.2 A/V
Proportional gain, $K_{\rm p}^{\rm i}$	2 V/A
Integral gain, $K_{\rm i}^{\rm v}$	12 A/Vs
Resonant gain, $K_{\rm i}^{\rm i}$	600 V/As
Resonant damping term, ζ	0.01
High-pass filter pole, a	15 rad/s

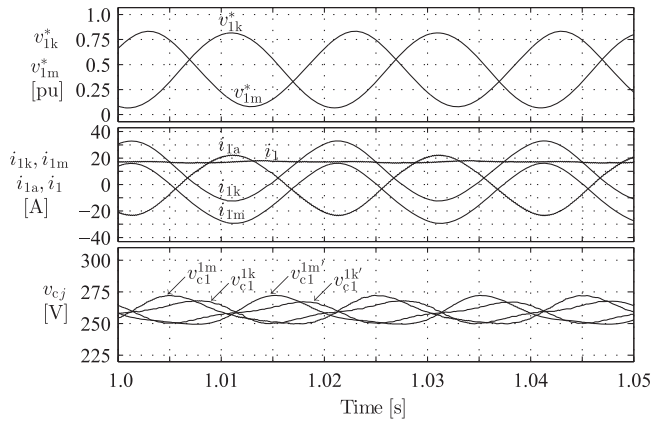

Fig. 11. Single-string architecture in Fig. 10 operating in step-down mode with $v_{\rm in} = 478$ V, $v_{\rm out} = 240$ V, $P_{\rm out} = 4.0$ kW; waveforms recorded using Linux-based data acquisition software with $f_{\rm sample} = 2f_{\rm sw}$.

adjusted to provide the desired input/output voltage ratio of 0.5 and nominal SM capacitor voltage of 260 V. The ac voltage $\hat{V}$ is set to achieve outer arms voltages of 94 $V_{\rm pk}$ (uncompensated); further details are provided in Section VI-C.

In Fig. 11, the positive pole ac modulating signals $\tilde{v}_{\rm 1k}^*, \tilde{v}_{\rm 1m}^*$ and positive pole ac arms currents $\tilde{i}_{\rm 1k}, \tilde{i}_{\rm 1m}$ exhibit similar phase relationships to those discussed for Fig. 8; namely, $\tilde{v}_{\rm 1k}^*$ and $\tilde{i}_{\rm 1k}$ are phase-shifted 180° while $\tilde{v}_{\rm 1m}^*$ slightly lags $\tilde{i}_{\rm 1m}$ as shown by Fig. 6(a). Positive pole SM capacitor voltages $v_{\rm c1}^{\rm 1k}, v_{\rm c1}^{\rm 1m}$ demonstrate the average ac power exchange from outer arm to inner arm ensures proper charge balancing. Negative pole SM capacitor voltages $v_{\rm c1}^{\rm 1m'}, v_{\rm c1}^{\rm 1k'}$ confirm the requisite ac power exchange also occurs between negative pole arms.

Experimental waveforms for the positive pole currents and input/output dc quantities are given in Fig. 12. Fig. 12(a) shows the switching ripple content which cannot be seen in the waveforms of Fig. 11. In Fig. 12(b), a small amount of ripple in $i_{\rm out}$ contains both 50 and 100-Hz components. The 50-Hz component is present because interleaving is not utilized. The 100-Hz component can be mitigated as discussed in Section V-B.

A key observation from Fig. 12(b) is that $i_{\rm in}$ is effectively free of 50-Hz ripple. Although further discussed in Section VI-C, this shows ac currents used for SM capacitor power balancing can be confined to circulate within the converter structure despite typical load and parameter imbalances. Such validation is largely important to demonstrate the practical feasibility of the proposed energy conversion concept for the DC-MMC.

B. Step-Up Operation

Fig. 13 shows experimental results for step-up operation with $v_{\rm in} = 478$ V, $v_{\rm out} = 500$ V, and $P_{\rm out} = 4.2$ kW. This experiment supplements the step-up scenario in Fig. 9, as both utilize voltage conversion ratios greater than unity. D is adjusted to achieve a voltage conversion ratio of 1.05 and nominal SM capacitor voltage of 325 V. The ac voltage $\hat{V}$ is set to achieve outer arms voltages of 35 $V_{\rm pk}$ (uncompensated).

Similar to Fig. 9, $\tilde{v}_{\rm 1k}^*$ and $\tilde{i}_{\rm 1k}$ are in phase while $\tilde{v}_{\rm 1m}^*$ lags $\tilde{i}_{\rm 1m}$ by nearly 180°. This reflects delivery of average ac power from inner arm to outer arm as dictated by Fig. 6(b). Note the average component of $i_{\rm 1m}$ is small relative to the average value of $i_{\rm 1k}$, which is consistent with the simulated step-up scenario. $v_{\rm 1k}^*$

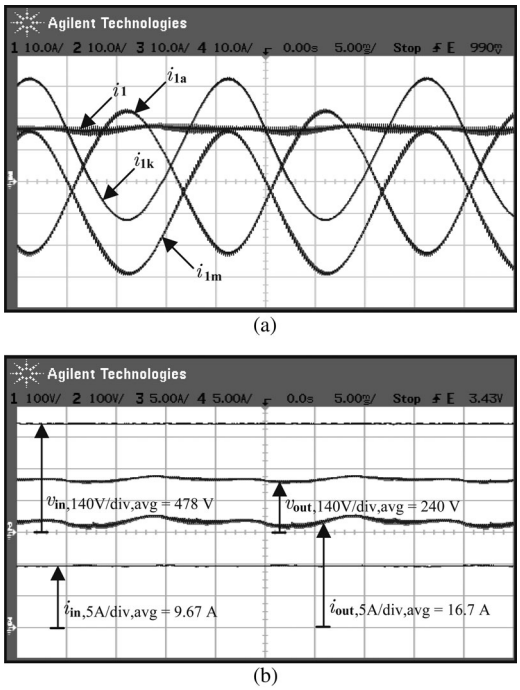

Fig. 12. Single-string architecture in Fig. 10 operating in step-down mode with $v_{\rm in} = 478$ V, $v_{\rm out} = 240$ V, $P_{\rm out} = 4.0$ kW; voltage channel gains are 140 V/div due to external sensor gain of 1.4 V/V: (a) positive pole currents (b) input and output dc quantities.

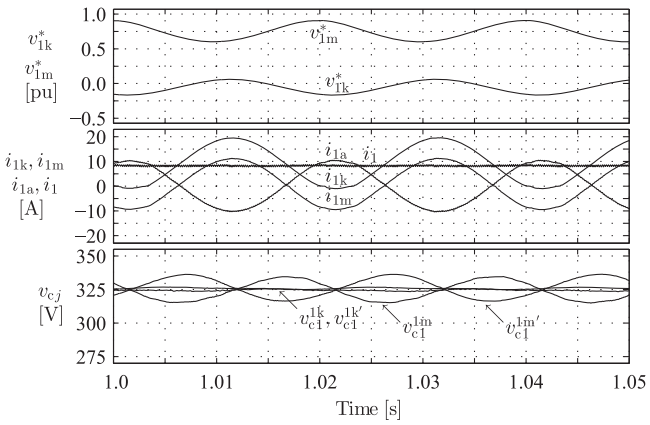

Fig. 13. Single-string architecture in Fig. 10 operating in step-up mode with $v_{\rm in} = 478$ V, $v_{\rm out} = 500$ V, $P_{\rm out} = 4.2$ kW; waveforms recorded using Linux-based data acquisition software with $f_{\rm sample} = 2f_{\rm sw}$.

illustrates the outer arm FB/SM injects the appropriate bipolar voltage as required for $D > 1$. The steady-state responses of $v_{\rm c1}^{\rm 1k}, v_{\rm c1}^{\rm 1m}, v_{\rm c1}^{\rm 1m'}, v_{\rm c1}^{\rm 1k'}$ verifies SM capacitor power balance can in practice be achieved for step-up operation using the open loop voltage control scheme in Fig. 7. SM capacitor voltage ripple for the inner and outer arms is 19.6 and 1.8 $\rm V_{pk-pk}$, respectively. The relatively large voltage ripple for the inner arms relative to the outer arms is consistent with Fig. 9.

DC input and output experimental waveforms are shown in Fig. 14. Similar to Fig. 12(b), these waveforms validate the practical feasibility of the proposed energy conversion concept

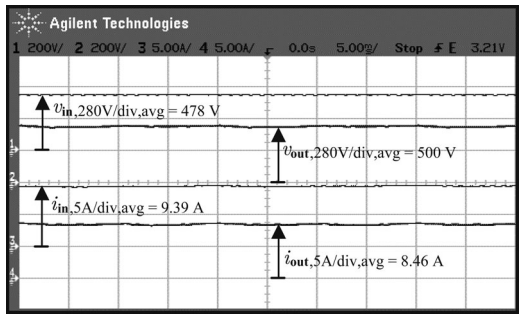

Fig. 14. Single-string architecture in Fig. 10 operating in step-up mode with $v_{\rm in} = 478$ V, $v_{\rm out} = 500$ V, $P_{\rm out} = 4.2$ kW; voltage channel gains are 280 V/div due to external sensor gain of 1.4 V/V.

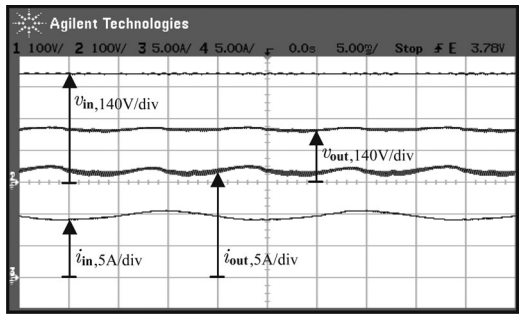

Fig. 15. Experimental result corresponding to Fig. 12(b) where 50 Hz ripple in $i_{\rm in}$ exists prior to its elimination via proposed compensation scheme.

as the circulating ac currents remain internal to the DC-MMC structure.

C. Practical Control Consideration: Pole Asymmetry

Due to practical aspects such as component variation, unequal device losses and pole loading imbalances, the experimental setup in Fig. 10(b) initially exhibited a small degree of asymmetry between poles. This asymmetry manifested itself by inciting a 50-Hz ripple in $i_{\rm in}$. That is, a small net fundamental frequency ac voltage component existed across the input dc rails of the converter, due to imperfect ac voltage cancellation along the string. Sources of imperfect cancellation include unequal circulating ac currents between poles, component variations between each $C_{\rm r}/2$, $L_{\rm r}$, $L_{\rm a}$, or load impedance imbalance. Such scenarios do not occur in simulation where ideal conditions are imposed. As an example, the impact of uncompensated pole asymmetry on the step-down experiment in Fig. 12(b) is illustrated by Fig. 15. Here, an undesired 50-Hz ripple component of $i_{\rm in}$ is seen to be 1.4 $\rm A_{pk-pk}$. To address this practical issue, an unutilized degree of control freedom was exploited.

To eliminate the 50-Hz ripple in $i_{\rm in}$, such as that shown in Fig. 15, a slight magnitude and phase adjustment was made to the 50-Hz component of $v_{\rm 1k}$. This strategy, conceptualized in Fig. 16, was implemented in Figs. 11–14. The key concept is that a small change in the 50-Hz component of $v_{\rm 1k}$ causes a corresponding change in the circulating ac current $i_{\rm 1a}$. By using the appropriate $\Delta\hat{V}$ and $\Delta\varphi$, the ac voltage drop across the positive pole $C_{\rm r}/2$ can be shifted to achieve zero net ac voltage along the entire string. Although implemented for the

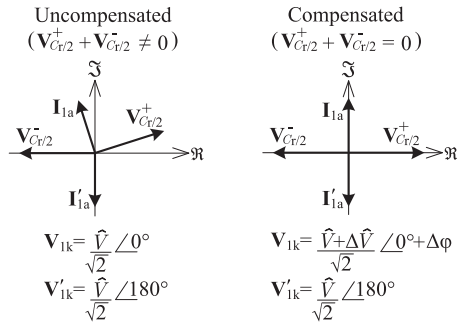

Fig. 16. Phasor diagrams illustrating adjustment to fundamental frequency component of $v_{1\mathrm{k}}$ in Fig. 10 to eliminate undesired ripple in i_{in}.

TABLE IV
UNCOMPENSATED VERSUS COMPENSATED 50 HZ COMPONENT OF $v_{1\mathrm{k}}$ IN FIG. 7 TO ELIMINATE 50 HZ i_{in} RIPPLE

50 Hz component of $v_{1\mathrm{k}}$		
Operating Mode	**Uncompensated**	**Compensated**
Step-down	$94.0\cos(w_{\mathrm{m}}t)$	$91.4\cos(w_{\mathrm{m}}t+5.3°)$
Step-up	$35.0\cos(w_{\mathrm{m}}t)$	$36.3\cos(w_{\mathrm{m}}t+5.5°)$

positive pole, this scheme is equally valid for the negative pole. Table IV lists the magnitude and phase adjustments used for the step-down and step-up experiments. Note only relatively small adjustments were required. These parameters were determined experimentally and added as fixed offsets to the control logic in Fig. 7. Although sufficient to demonstrate efficacy of this compensation method, in practice closed loop regulation can be readily developed based on the concept of ac voltage adjustment.

VII. CONCLUSION

A new modular multilevel dc/dc converter, termed the DC-MMC, is presented for the interconnection of bipolar HVDC networks. The DC-MMC features a new class of bidirectional single-stage dc/dc converters utilizing interleaved strings of cascaded SMs. Power balance for each SM capacitor is achieved via circulating ac currents, which are established by reactive elements linking each string.

The two-string and three-string architectures for the DC-MMC are introduced, where the latter shows similarity to the three-phase dc/ac MMC structure. In general, an arbitrary number of strings can be interleaved. By employing a unique arrangement of HB/SMs and FB/SMs for each string, the DC-MMC can provide both step-up and step-down operations and interconnect HVDC networks of similar voltage levels. Moreover, the utilization of a sufficient number of cascaded FB/SMs in the outer arms enables bidirectional fault blocking capability similar to a dc circuit breaker.

A simplified model of the converter strings is presented and the ideal dc/dc conversion process is analyzed in detail. An open loop voltage control scheme is proposed for the single-string and two-string architectures that adopts closed-loop ac current control to maintain power balance of the SM capacitors. The proposed scheme has the benefits of minimizing the circulating ac currents needed for the dc/dc conversion process while significantly reducing the installed circuit reactance. As an adopted case study, a switched model of the two-string architecture is implemented in PLECS to validate the DC-MMC operation. Experimental results from a 4-kW prototype, which is based on a single-string implementation of the multistring architectures, further validate the ability to maintain power balance of SM capacitors by way of circulating ac currents. The experimental work demonstrates that the DC-MMC offers sufficient control freedom to compensate for load and parameter imbalances as would be expected in any field installation.

APPENDIX

The output filters in Figs. 1 and 2 consist of passive elements L_{f} and C_{f}. Basic design guidelines for the coupled inductor L_{f} are provided. These guidelines consist of dc and ac voltage and current ratings for sizing of the coupled inductor. Requirements for the filter capacitor are not detailed here as C_{f} is sized simply to carry switching harmonics.

Each coupled inductor in Figs. 1 and 2 must be rated to handle the maximum rms voltage imposed across the windings and the maximum rms current carried by the windings. The maximum rms voltage across each winding of a coupled inductor is

$$(V_{\mathrm{f}}^{\max})_{\mathrm{rms}}=\frac{\hat{V}^{\max}}{\sqrt{2}} \tag{13}$$

where $\hat{V}^{\max}$ is the maximum peak ac voltage synthesized by the outer arms (see Fig. 6).

The maximum rms current carried by each winding of a coupled inductor can be approximated as

$$(I_{\mathrm{f}}^{\max})_{\mathrm{rms}}\approx\frac{i_{\mathrm{in}}^{\max}}{nD} \tag{14}$$

where $i_{\mathrm{in}}^{\max}$ is the maximum DC-MMC input current. The rms quantity (14) assumes the winding current is dominated by its dc component (see Fig. 4), which relies on L_{f} being sufficiently high to provide adequate ac output filtering. The simulations in Section V and experimental work in Section VI show this to be a reasonable approximation.

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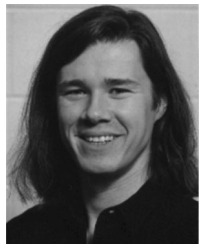

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